Supercomputing in Japan

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Generations

- Primordial Ages (1970's)
  - Cray-1, 75APU, IAP
- 1st Generation (1H of 1980's)
  - Cyber205, XMP, S810, VP200, SX-2
- 2nd Generation (2H of 1980's)
  - YMP, ETA-10, S820, VP2600, SX-3, nCUBE, CM-1
- 3rd Generation (1H of 1990's)
  - C90, T3D, Cray-3, S3800, VPP500, SX-4, SP-1/2, CM-5, KSR2（HPC ventures went out）
- 4th Generation (2H of 1990's)
  - T90, T3E, SV1, SP-3, Starfire, VPP300/700/5000, SX-5, SR2201/8000, ASCI(Red, Blue)
- 5th Generation (1H of 2000's)
  - ASCI，TeraGrid，BlueGene/L，X1, Origin,Power4/5, ES, SX-6/7/8, PP HPC2500, SR11000, ….

Primordial Ages (1970's)

1974	DAP, BSP and HEP started	
1975	ILLIAC IV becomes operational	
1976	Cray-1 delivered to LANL	80MHz, 160MF
1976	FPS AP-120B delivered	
1977	FACOM230-75 APU	22MF
1978	HITAC M-180 IAP	
1978	PAX project started (Hoshino and Kawai)	
1979	HEP operational as a single processor	
1979	HITAC M-200H IAP	48MF
1982	NEC ACOS-1000 IAP	28MF
1982	HITAC M280H IAP	67MF

Characteristics of Japanese SC’s

1. Manufactured by main-frame vendors with semiconductor facilities (not ventures)
2. Vector processors are attached to mainframes
3. HITAC IAP

   a) memory-to-memory

   b) summation, inner product and 1st order recurrence can be vectorized

   c) vectorization of loops with IF’s (M280)
4. No high performance parallel machines

1st Generation (1H of 1980's)

1981 FPS-164 (64 bits)

1981 CDC Cyber 205 400MF

1982 Cray XMP-2 Steve Chen 630MF

1982 Cosmic Cube in Caltech, Alliant FX/8 delivered, HEP installed

1983 HITAC S-810/20 630MF

1983 FACOM VP-200 570MF

1983 Encore, Sequent and TMC founded,

ETA span off from CDC

1st Generation (1H of 1980's)
(continued)

1984 Multiflow founded
1984 Cray XMP-4 1260MF
1984 PAX-64J completed (Tsukuba)
1985 NEC SX-2 1300MF
1985 FPS-264
1985 Convex C1
1985 Cray-2 1952MF
1985 Intel iPSC/1, T414, NCUBE/1, Stellar, Ardent…
1985 FACOM VP-400 1140MF
1986 CM-1 shipped, FPS T-series (max 1TF!!)

Characteristics of Japanese SC in the 1st G.

1. Compatibility with the mainframes
   (S and VP are IBM compatible)
2. Single processor, multiple pipes
3. Large main memory (256MB vs. XMP 32MB)
4. Large vector registers
5. List-directed vector instructions (gather/scat)
6. Different control of vector units
7. No commercial parallel machines

2nd Generation (2H of 1980's)

1987 ETA-10 10GF(max)
1987 CM-2
1987 Steve Chen left Cray to found SSI
1987 HITAC S-820 3GF(max)
1988 Cray YMP 4GF(max)
1988 Intel ipsc/2
1988 MasPar founded, Tera Computer founded
1989 ETA shut down, JvN SC shut down
1989 Seymour left Cray to found CCC

2nd Generation (2H of 1980's)
(continued)

1989 BBN TC2000, Myrias SPS-2, Meiko CS, NCube2

1989 FACOM VP2600 5GF(max) 2 proc.

1989 ES-1 delivered and shut down after 2 sells

1990 MITI Supercomputer Project ended 10GF

1990 Intel ipsc/860, MasPar MP-1

1990 NEC SX-3 22GF 4 proc.

1990 QCDPAX completed (Tsukuba) 432 proc.

1988 First Supercomputing Conference in Orland

Characteristics of Japanese SC in the 2nd G.

1. Vector multiprocessor appeared in Japan
   with modest multiplicity 2-4 vs. 8 (YMP, ETA)
2. The technology developed for the vector is transferred to mainframes
   (Used to be: mainframe→vector)
3. Still no commercial MPP's in Japan

3rd Generation (1H of 1990's)

1991 Cray Y/MP C90 16 proc. (max)
1991 Kendall Square Research started
1991 Myrias, Stardent shut down
1991 Intel Paragon, CM-5
1992 FPS bankrupt (server section went to Cray)
1992 MasPar MP-2
1993 Cray T3D, CS6400, nCUBE2, KSR1
1993 SSI shut down
1993 HITAC S-3800 32GF(max) 4 proc.

3rd Generation (1H of 1990's)
(continued)

1993 Fujitsu installed NWT in NAL 140 proc.
Fujitsu VPP500 222 proc. (max)

1993 IBM SP-1 announced and delivered

1993 Cray-3 installed in NCAR 4 proc.

1993 NEC Cenju-3 256 proc.(max)

1994 SP-2, Cray-4 announced

1994 Fujitsu AP1000 1024 proc. (max)

1995 NEC SX-4 1TF(max) 512 proc.

1995 CCC bankrupt

Characteristics of Japanese SC in the 3rd G.

Drastic changes in Japanese vectors

1. Hitachi
   Shared memory vector parallel processor
   using ECL technology
2. Fujitsu
   Distributed memory vector parallel proc.
   using GaAs as well as silicon tech.
3. NEC
   Cluster of shared memory vector parallel
   Unix as host OS

◆ Commercial MPPs, sold as a parallel testbed

4th Generation (2H of 1990's)

1995 Cray T90 16GF(max)

1995 Fujitsu VPP300 CMOS 2.2GF/PE max16

1996 cp-pacs (Tsukuba) first 300, in autumn 600 GF

1996 Cray T3E delivered

1996 Hitachi SR2201 CMOS 300MF/PE max 2048
(pseudovector on PA-RISC)

1996 Fujitsu VPP700 max 256

1996 Cray merged in SGI after selling Chippewa works
Superserver went to Sun (Enterprise)

4th Generation

1996 Seymour Cray died after car accident (Oct.)
1996 Fujitsu AP3000
1997 NEC Cenju-4
1997 ASCI Red (Intel) 1.8TF
1998 Cray SV1 CMOS 4GF/PE
1998 Hitachi SR8000 8GF/node max 128
(pseudovector on Power arch.)
1998 ASCI Blue Pacific (IBM), Mountain (SGI)
1998 NEC SX-5 CMOS 8GF/PU max 512

Characteristics of Japanese SC in the 4th G.

1. Fujitsu and NEC seem to follow the line of conventional vector supercomputers

    Fujitsu: distributed memory

    NEC: cluster of shared memory nodes

2. Hitachi adopted RISC (pseudo)vector arch.

    SR8000: 8 CPUs in one node

Fifth Generation

- 2000: ASCI White (LLNL, IBM) 12 TF
- 2002: ASCI Q (LANL, HP/Compaq/DEC) 20TF
- 2004: Thunder (LLNL) 23TF
- 2004: TeraGrid
  - SDSC, CalTech, NCSA, ANL, Pittsburgh, ….
- 2004: BlueGene/L prototype (LLNL) 16TF
- 2004: NASA Columbia (SGI) 64TF?
- 2004: BlueGene/L at IBM 90TF

Fifth Generation

- 2000: SGI sold Cray division to Tera, which is renamed as Cray Inc.
  - 2002：X1
  - 2004: XD1
- SGI
  - 2001: Origin3800
  - 2002: Origin3900
- IBM
  - 2001: eServer p690 (Regatta)
  - 2003: Power 5
- Sun
  - 2001: Sun Fire15000

Fifth Generation (Japan)

- NEC
  - 2002: Earth Simulator (40TFlops)
  - 2002: SX-6
  - 2003: SX-7
  - 2004: SX-8
- Fujitsu
  - 2002: PRIMEPOWER HPC2500
- Hitach
  - 2004: SR11000

Overview

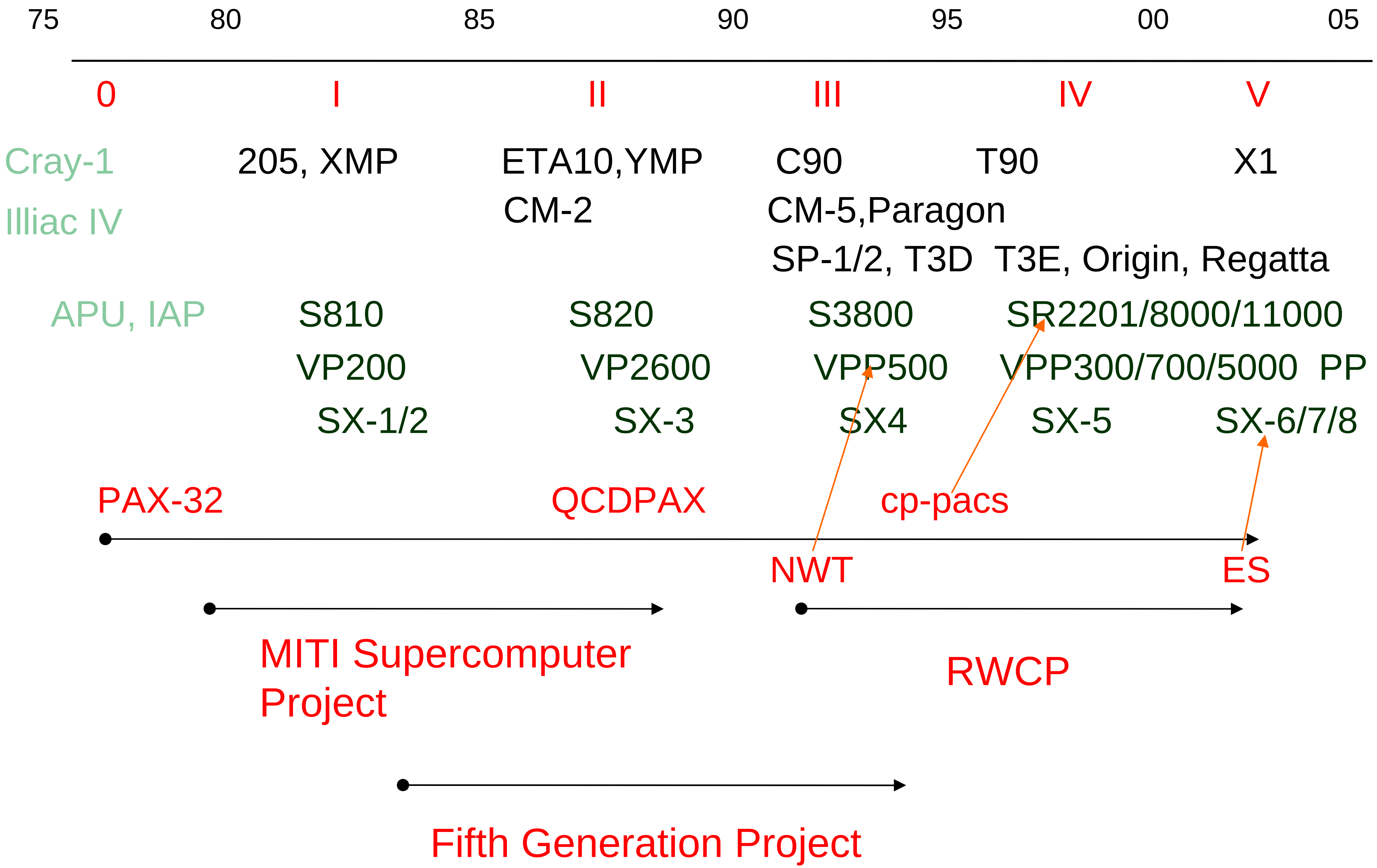
1. Cray vectors were for professionals
   Japanese vectors were for novices.
2. Japanese vectors were designed as an extension of mainframe computers.
3. Japanese vendors are big semiconductor producers and have high density packaging capabilities.

Overview (continued)

4. Research induced machines were commercialized:

NWT	VPP500/300/700/5000
cp-pacs	SR2201/8000
Earth Simulator	SX-6/7/8

5. Limited experience of COTS parallel machines
6. Can vectors survive?
7. Application Software!!!!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05
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I
II
III
IV
V
Cray-1
Illiac IV
205, XMP
ETA10,YMP
CM-2
C90
CM-5,Paragon
SP-1/2, T3D
T90
T3E, Origin, Regatta
X1
APU, IAP
S810
VP200
SX-1/2
S820
VP2600
SX-3
S3800
VPP500
SX4
SR2201/8000/11000
VPP300/700/5000
PP
SX-5
SX-6/7/8
PAX-32
QCDPAX
cp-pacs
NWT
ES
MITI Supercomputer Project
RWCP
Fifth Generation Project

From dedicated computers to commercial products

- Expertise from universities and government labs to industry
- Continued support from the industry of the dedicated machines
- Ecosystem: dynosaurus cannot live alone!
- In US: cosmic cube to Intel ipsc/1

  QCDOC to BG/L?

  Redstorm to XT3

京 速 計算機

Kei *Soku* *Keisanki*

10^{16} speed computer

Formal Title:

“Development of most advanced high-performance general-purpose supercomputer”

Notice

- This talk is based on those open materials
  - Newspapers
  - Web news
  - Mext (Ministry of Education, Culture, Sports, Science and Technology) Web pages
  - Open symposiums
- Many figures are taken from Mext pages. Sorry for Japanese captions!!

  (http://www.mext.go.jp)

Project Proposal

- Seven-year plan (2006-2012) of $1B (total) .
- Leadership of Japan in supercomputing----simulation, data mining, analysis.
- Outline
  - Design and development of software (OS, middleware, applications)
  - Design and development of hardware (10 PF system, interconnection)
  - Advanced Center for Computational Science and Technology

Current Status

- R&D of element technologies in process (2005-2007)
- Semi-official announcement of 10 PF supercomputer development project (the machine will be ready in 2010fy)
  - July 25, 2005
- Mext submitted the budget proposal for 2006fy to MoF at the end of August
- CSTP endorsed the project with comments (I was in the evaluation subcommittee of the CSTP)

Current Status

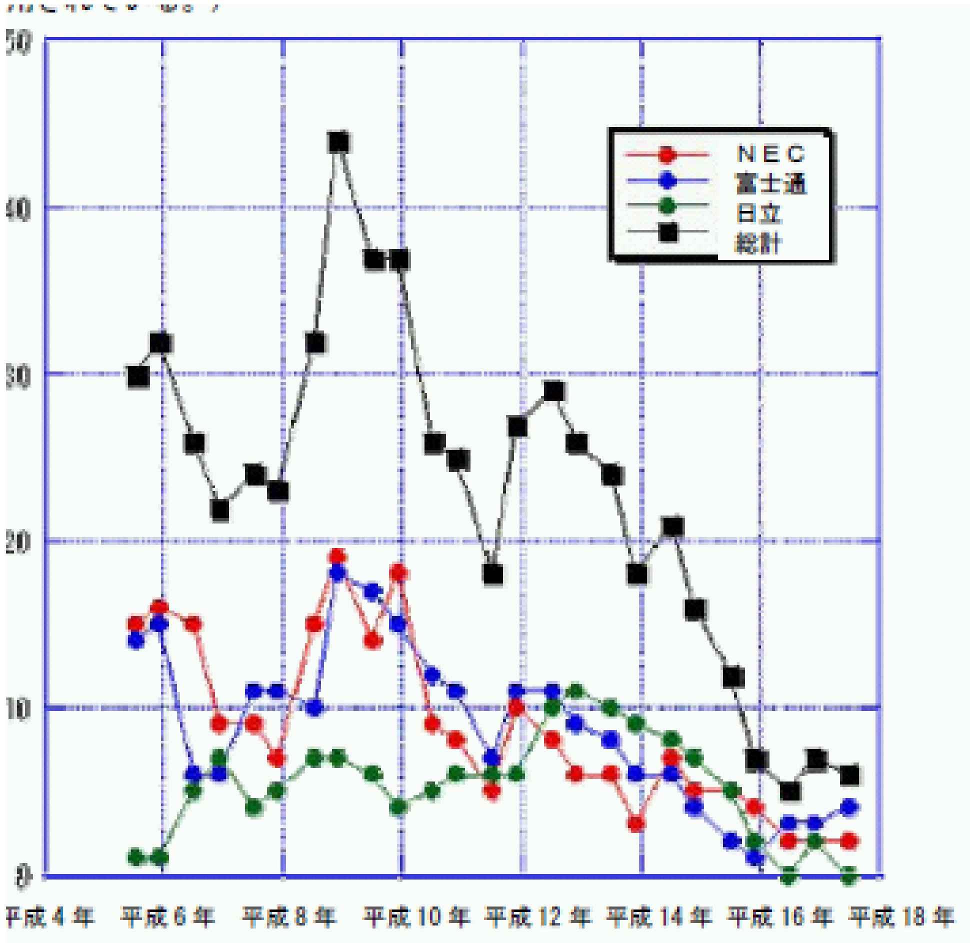
- The project was accepted by Parliament for 2006fy ($30+M)
- Leaders
  - Project leader: Dr. Tadashi Watanabe (<NEC)
  - Sub-leaders (part time): Prof. Ken Miura (NII, <Fujitsu), Prof. Shun Kawabe (Meisei U, <Hitachi), Dr. Toshikazu Takada (NEC Lab.)
  - Dr. Ryutaro Himeno leads Riken team.

Background

Japanese Machines in Top 20

	9306	9311	9406	9411	9506	9511	9606	9611	9706	9711	9806	9811	9906	9911	0006	0011	0106	0111	0206	0211	0306	0311	0406	0411	0506	0511	
1		NWT		NWT	NWT	NWT	Todai	cp-p											ES	ES	ES	ES	ES				
2			NWT				NWT	NWT	cp-p																		
3								Todai	NWT															ES			
4									Todai	cp-p			Todai												ES		
5	NEC		ATP	ATP	KEK	KEK								Todai	LRZ		Todai										
6	AES	NEC	Tsuku	Tsuk						Todai	cp-p				KEK						NAL					ES	
7		AES	Riken	Riken	JAERI		KEK			NWT						LRZ		Todai					Riken				
8								KEK		ECMW							Osak								AIST		
9						NEC		Kyush							Todai	KEK											
10			Hitach	Hitac			NEC	ECMW																			
11			Todai	Todai		JAERI	Stutt															JAXA					
12			NEC			Nagoy					AES		TAC			ECMW	LRZ	Osak								AIST	
13			Toho								Toho					Todai			Todai								
14					ATP	Gene	JAERI				Todai	cp-p					KEK		LRZ					Riken			
15				AES	Tsuk	ISS	Nagoy				NWT			Kyoto											JAERI		
16				NEC	Riken												ECMW										
17			Toho	Toho			Gene	NEC	Kyush					TAC	ISS		Todai	LRZ									
18			AES	Toho			ISS	Osaka	KEK			AES	cp-p			JMA											
19			IMS	AES		ATP		Osaka			ECMW	FZJ						KEK	Osak								
20				IMS		Tsuk		Stutt															AIST				

Japanese Machines in Top100



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Developments in China

- On July 12, the president of Dawning Group(曙光集团) said:
  - Dawning 5000 (5th generation) will attain 100 TF
  - The 6th generation supercomputer will attain 1000 TF
  - In collaboration with CAS
  - They are developing their original CPU *Long Xin*（龍芯, Dragon Core）for Dawning 5000.
  - The 6th generation machine will use more *Long Xin* chips.

Developments in China

- Lenovo Group（聯想集団）announced July 28:
  - It is developing a 10 times more powerful supercomputer than the current world fastest.
  - Lenovo supercomputer will attain 1000 TFlops
  - It is expected to be completed during China’s 11th five-year plan (2006-2010).

Preparations in Japan

- Information Science and Technology committee in Mext has been discussing the measures to promote computational science and technology since August 2004.
- Mext funded four projects to promote “Element Technologies for Future Supercomputers” in 2005-2007.

R&D of Element Technologies for Future Supercomputing

- Three year project (2005-2007fy)
- Four groups were accepted
  1. System Interconnect (Kyushu U and Fujitsu)
  2. Interconnect by IP (U of Tokyo, Keio U etc)
  3. Low Power Device and Circuits (Hitachi, U of Tokyo, U of Tsukuba)
  4. Optical Connection of CPU and Memory (NEC and Titech)

– $40M per year (in total)

Interim Report of Computational Science and Technology WG in Mext

Killer Applications
Grand Challenge

- Industrial Design
- Nanotechnology
- Disaster Prevention
- Atomic Energy
- Life Science
- Climate and Environment
- Space and Aeronautics
- Astrophysics and Space Science

広汎な分野での利活用　－ 次世代スパコンが拓く世界 －

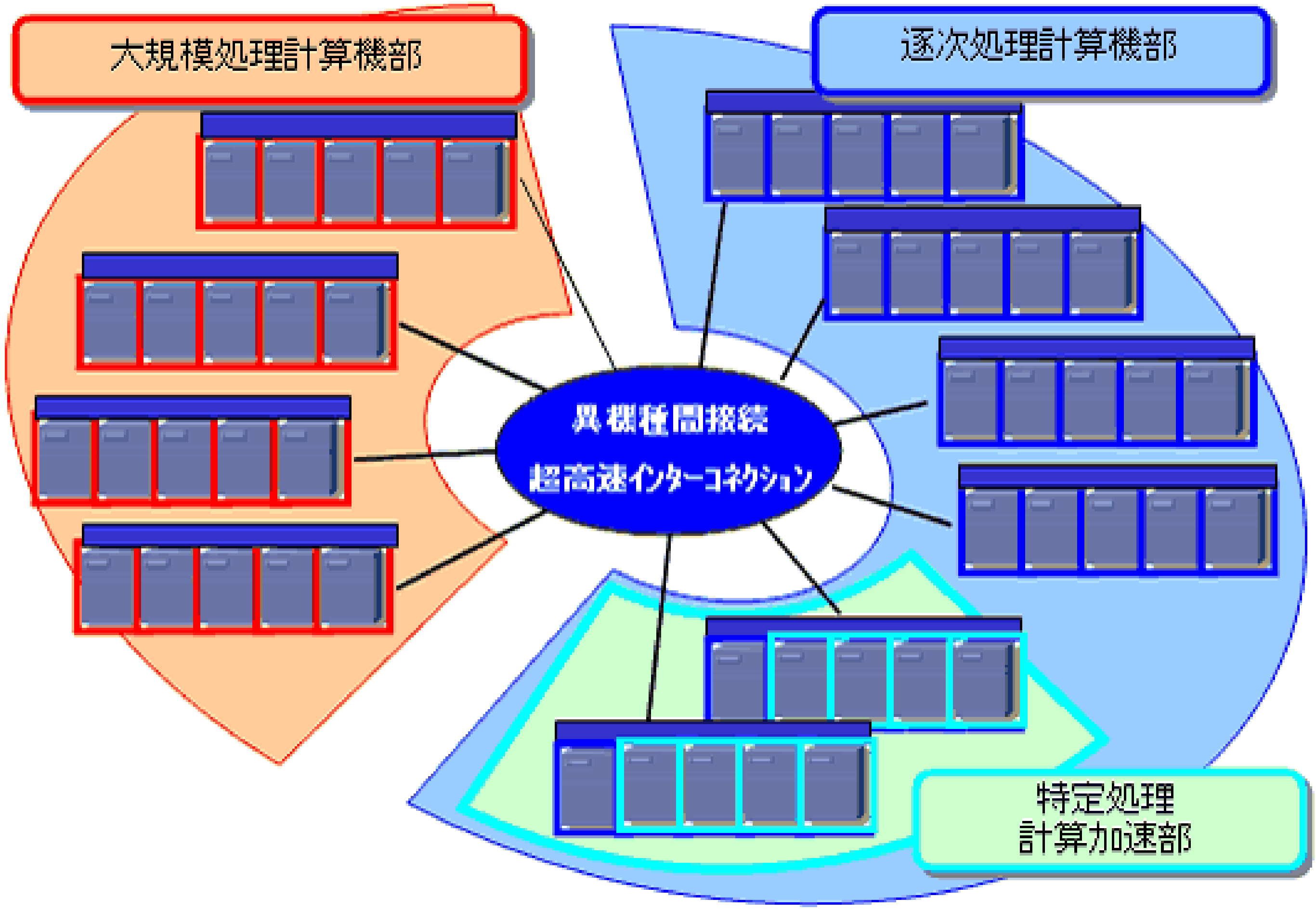
Observations of the WG

- Multiphysics multiscale simulation will be important in those fields.
- To keep high performance in different types of computing, hybrid architecture will be appropriate.
- The connection between different architectures should have high speed.

Architecture Sketch

Large scale processing

Scalar computer



Special-purpose computer

Requirements from these Applications

1. Large-scale processing part
   - Although never explicitly stated, this part is believed to be a vector/pseudovector computer.
   - 2 PF from disaster prevention
     1 PF from drug design
     0.2-0.6 PF from various fields

Requirements from these Applications

2. Scalar computer part
   - 4 PF from device simulation with electron correlation
   - 0.3-0.5 PF from various fields
3. Special purpose computer
   - 20 PF from drug design (MD)
   - 20 PF from astrophysics

The architecture is NOT yet decided.

My Personal View

Why vector?

- There is a strong arguments to include vector architecture in the 10 PFlops machine.
  1. Vector computer is easy to program and can get high efficiency in large class of problems.
  2. Japan has a unique potential to construct high performance vector machines and this potential should be fostered.
  3. National project should promote what is not a commodity.

However!

1. The vector performance is attained by large memory BW (0.5word / flop). It is unrealistic in PFlops region.
   – Number of gates, connections
   – Power and heat
   – Budget (price-performance ratio)
2. World trend is against vector.
3. Should we make effort to save the endangered species?
4. Technology which does not lead to commodity cannot live.

Really Usable Machine?

- *Kei-Soku* machine is proposed as a general-purpose system.
- Pruned architecture design is feasible only when confronted with a few target programs.
  - NWT for aerodynamics, cp-pacs for QCD and ES for atmospheric eq.
- Those machines became multi-purpose system eventually.
- Current plan is a collection of technologies of three main-framers. It looks like a pork-barrel budget.

Architecture-Application Co-design

- Two kinds of "maniacs" (*Otaku*)
  - Computer maniacs: they want to build high performance machines anyway and they invite users after that.
  - Application maniacs: they are ready to tune their codes once a computer is provided.
- Any of the two is not appropriate to *Keisoku* design. Co-design is crucial.
- *Baramaki* (pork-barrel) is out of the question.

Can it make Japanese HPC industry stronger?

- Some government supported projects produced commercialized products:
  - NWT (STA) VPP500/300/700/5000
  - cp-pacs (MoE) SR2201/SR8000
  - ES (STA) SX-6/7/8
  - RWCP (MITI) clusters
- Some did not:
  - Japanese supercomputer project 1981-89 (10GF machine, MITI)
  - 5th generation project (MITI)

Not a single-shot project

- To make only one top machine is not enough. Appropriate cyber-infrastructure should be provided for researchers and developers.
  - From top to bottom (hierarchical)
- Constant research investment with a roadmap is important. Although follow-up projects are proposed in the report, there is no approved long-term roadmap for supercomputing in Japan.
  - NWT, cp-pacs and ES were actually single-shot events.

Concluding Remarks

- Japan has developed supercomputers since 1977
- Japanese vector computers were designed as an extension of main frames.
- Development cost was amortized among mainframes.
- Stress of easiness of use (compilers and tools).
- Late entry to parallel architectures
- Influence of research project machines.
- Loss of dominance in high-end machines.

Concluding Remarks

- Mext will start 10 Peta Flops project for 2006-2010fy.
- More severe arguments are necessary to make it a really usable infrastructure for computational science and technology.
- It is not easy that the coming machine may get the No.1 in the world ranking (Top500 or HPCC or what).